IN THE CLAIMS

1. (Original) A semiconductor integrated circuit device comprising:

a plurality of memory cells each of which includes a capacitor and has a voltage input node and a storage node at opposite sides of the capacitor, respectively;

a first voltage generating circuit for generating a first voltage;

a second voltage generating circuit for generating a second voltage lower than the first voltage; and

a switching circuit which receives the first and second voltages and changes over the first and second voltages in response to a control signal so as to output the first and second voltages to the voltage input node in a normal operation mode and a data retention test mode, respectively.

2. (Original) The semiconductor integrated circuit device according to Claim 1, wherein the second voltage generating circuit is formed by a ground power source.

3. (Original) The semiconductor integrated circuit device according to Claim 1, further comprising:

a control circuit for generating the control signal;

wherein the control circuit includes a voltage detecting circuit for detecting a supply voltage in the data retention test mode so as to output a voltage signal indicative of the supply voltage, a standby signal generating circuit for generating a standby signal indicative of a standby state in the data retention test mode and a logic circuit for performing logic operation of at least the voltage signal and the standby signal.

4. (Currently Amended) The semiconductor integrated circuit device according to Claim 3, wherein the control circuit further includes a test mode signal generating circuit for generating a test mode signal indicative of the data retention test mode and the logic circuit is formed by a 3-input ~~3-inut~~ NAND gate for performing logic operation of the voltage signal, the standby signal and the test mode signal.

5. (Original) The semiconductor integrated circuit device according to Claim 1, wherein each of the memory cells includes a pair of bit lines, a word line traversing the bit lines, a pair of access transistors disposed between the bit lines such that each of the access transistors is connected between each of the bit lines and the storage node and has a gate connected to the word line, a pair of the capacitors each connected to a junction of each of the access transistors and the storage node, a pair of load transistors each connected between a power source and the storage node and a pair of driver transistors each connected between the storage node and ground such that a gate of each of the load transistors is connected to a gate of each of the driver transistors.